

Personas:

The customers of technology devices, products and services

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Fictional Persona Cast:

Max Smart ❖ *Chief Technology Officer*

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Laura Peterson ❖ *Technology Office Manager*

Tim Benkowski ❖ *Engineering Manager*

Maddie Olsen ❖ *Software Engineer*

David Chen ❖ *Architect*

Patrick Smith ❖ *Implementation Engineer*

Ravi Shukla ❖ *Verification Engineer*

Peter Branson ❖ *Board Designer*



Overview: Why Personas?

What are Personas?

Fictional characters representing real users that have personal behaviors and goals

Scenarios:

- Challenges, User Stories, Job Goals, Narrative

Why do we use personas?

- It's easier to build a successful online user experience if users' needs and goals are defined
- Build understanding and empathy
- Validates User Experience and User Interface design decisions
- Align company with agreed-upon personal profiles to focus on marketing, interactivity and messaging

Why now?

- Personas add the customer's viewpoint to the UX design process.
- A positive user experience is critical for successful online enterprises or ecommerce Web sites and mobile apps.



How We Use Personas?

Specific Persona Usage for Company Marketing

Usability Testing

- Identify scenarios and detailed tasks
- Recruit usability test subjects based on personas

Interactive Design

- Design for a specific persona who has a specific task

Writing

- Write for a specific persona who has a specific need

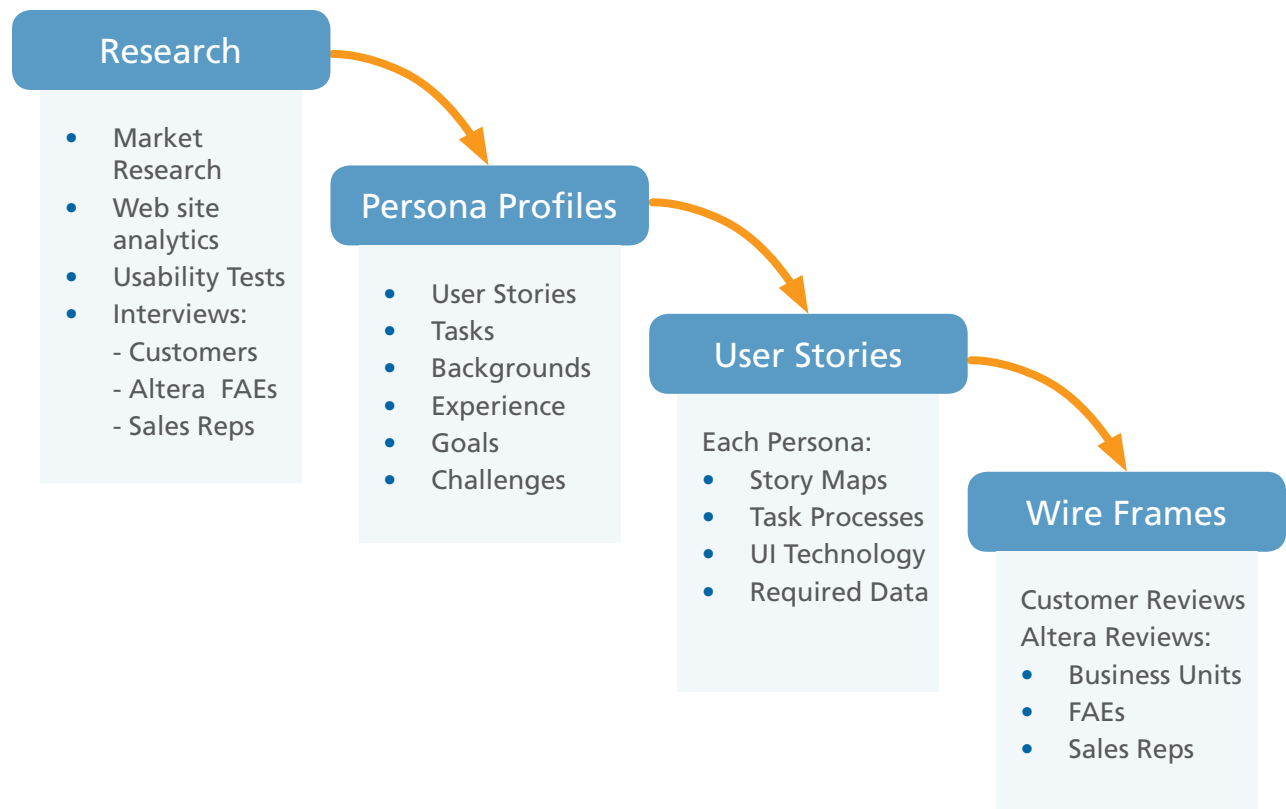
Marketing campaigns

- Targeted marketing to specific personas

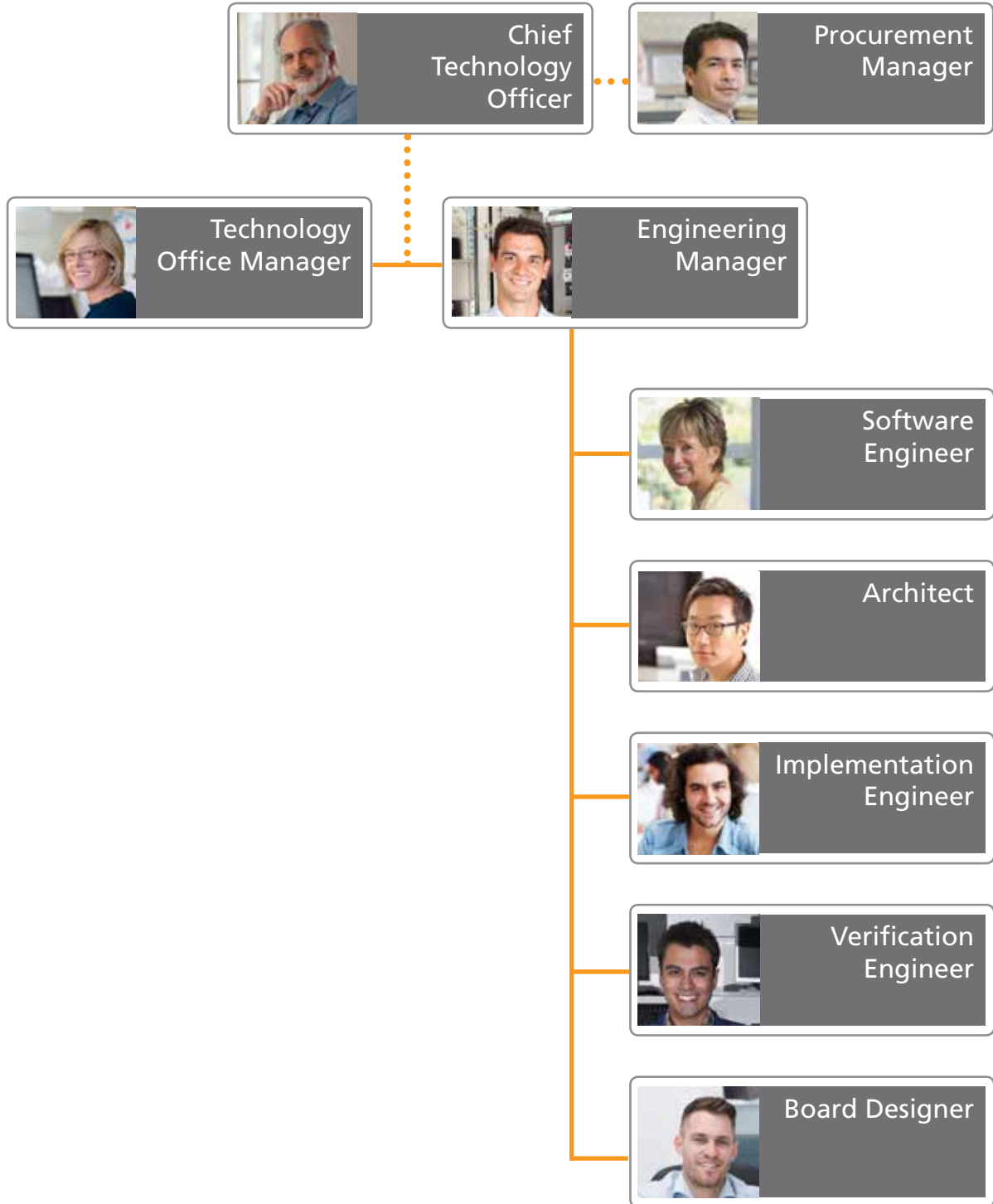
Most important

- Align company goals with users' goals

Persona Integration with UX Design Process



Organization Chart: Technology Customer Personas



Max Smart



Job Title: Chief Technology Officer
 Reports to: CEO or President

User Role: Executive
 Group: Senior Management

Decision Influence

- Decision Maker
- Veto Power
- Influencer

* Most influential users.

| Max | | | |
|---------|---|--|---|
| James | | | ● |
| Laura | | | ● |
| Tim* | ● | | |
| David* | ● | | |
| Maddie | ● | | |
| Patrick | ● | | |
| Peter | ● | | |

Challenges

- Purchases and contracts align with company goals
- Competitive position and the level of risk
- Saving time and money
- Competitive impact, ROI

User Stories

- I need to know high-level vendor and supplier information, such as BoD members, SEC filings, press releases
- I am interested in a vendor's case studies and how they solve problems
- I want to know a vendor's technology road map for future markets
- I need information on a vendor's warranties and exchanges

Job Goals

- Must create the company technology road map and understand dependencies on vendors and suppliers

Narrative

- Meet with vendors face-to-face for information
- Visionary: looking 3-5 years into the future
- Involved in the buying cycle very early and/or very late

Trust Relationships

- Industry peers and analyst social networks, management team and colleagues
- Live events, seminars and technical IEEE conferences
- Delegated offline and Web-based trials and demos

James Riviera



User Role: Purchasing
Group: Finance

Job Title: Procurement Manager
Reports to: CFO

Decision Influence

- Decision Maker
- Veto Power
- Influencer

* Most influential users.

| | | | |
|--------------|---|---|---|
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| David* | ● | | |
| Maddie | ● | | |
| Patrick | ● | | |
| Peter | ● | | |

Challenges

- Saving money and getting concessions from vendors
- Implement best practices for vendor management
- Mitigate vendor risk (diversification of vendors)

User Stories

- I need to find a vendor's latest press releases and product announcements
- I want to see a vendor's financials for the last quarter
- Is there any information on a vendor's current sales and sales projections?
- I need warranty and exchange information for every supplier product we purchase

Job Goals

- Project manage supplier and vendor activities and drive purchasing strategy and vendor policy
- Develop and monitor vendor performance metrics and scorecards, regularly analyzing and reporting on progress against strategic organization goals

Narrative

- Bachelor's or Master's degree in Supply Chain Management, Finance, Business or related field, maybe technical.
- CPM (Certified Purchasing Manager) credential
- Electronic procurement experience of ASICs and FPGAs
- Negotiation skills and contract management experience, knowledge of purchasing processes and tools

Trust Relationships

- Speaks to VP of Business Units, CAB, or Sales

Laura Peterson



Job Title: Technology Office Manager
Reports to: CTO

Decision Influence

- Decision Maker
- Veto Power
- Influencer

* Most influential users.

User Role: Manager
Group: Technology Group

| | | | |
|--------------|---|---|---|
| Max | | | ● |
| James | | ● | |
| Laura | | ● | |
| Tim* | ● | | |
| David* | ● | | |
| Maddie | ● | | |
| Patrick | ● | | |
| Peter | ● | | |

Challenges

- Creating and updating vendor scorecards
- Managing vendors
- Staying within a budget
- Prevent blind decisions based on technology, not the application
- Conducting vendor inspections

User Stories

- I need to find exact technology specifications for our vendor devices
- I have to be informed about recalls, and warranties
- I am looking for information I can use for evaluations, performance, cost vs. performance evaluations, and reliability testing

Job Goals

- Develop an approved vendor list, based on engineering evaluations and on scorecards
- Rank and rate vendors against each other
- Create standards for different levels of product requirement

Narrative

- Part of a central services management group
- Could be in finance, purchasing, quality assurance, or in a technical capacity
- Technical degree from a prestigious university
- Organized and efficient on the job with related work experience and training.

Trust Relationships

- Relies upon both the CTO and Engineering Manager for accurate product requirements
- Good relationships with subordinate coworkers

Tim Benkowski



User Role: Manager
Group: Technology Group

Job Title: Engineering Manager
Reports to: Director or VP of Engineering

Roles in Product Development Process

| Person | Requirements | Architecture | Implementation | Verification | Release |
|---------|--------------|--------------|----------------|--------------|---------|
| Tim | High | Low | Low | Low | High |
| Maddie | Low | High | High | High | Low |
| David | Low | Low | High | Low | Low |
| Patrick | Low | Low | Low | High | Low |
| Ravi | Low | Low | Low | Low | High |
| Peter | Low | Low | Low | Low | High |

Challenges

- Productivity; develop and produce new products, and manage multiple projects
- Managing global teams and low-cost development centers
- Shrinking development schedules and limited staff—more, faster for less
- Development efficiency and maintain quality in IP and supporting software

User Stories

- I need to find detailed product information quickly I can use for reports and presentations
- I want to know about related system designs I can use to compare my team's design against their peers and competitors.
- I need the same for reference designs

Job Goals

- Complete and deliver final products on budget and on schedule
- Influence and lead product feature development
- Major influencer in technology decisions
- Experience on existing and previous projects recognized and validated for future product road maps

Narrative

- Knowledgeable about end market system designs and applications
- Experienced with ASIC and/or FPGA designs
- Has limited and outdated design software experience for FPGA devices
- BSEE and post-graduate degree
- Manages a team of engineers

Trust Relationships

- Meets with FPGA vendors throughout design cycles
- Gets information from peers, vendor web sites, and Google searches
- Relies on vendor's track record and road map

Maddie Olsen



User Role: Engineer
Group: Technology Group

Job Title: Software Engineer
Reports to: Engineering Manager

Roles in Product Development Process

| | Requirements | Architecture | Implementation | Verification | Release |
|---------|--------------|--------------|----------------|--------------|---------|
| Tim | | | | | |
| Maddie | | | | | |
| David | | | | | |
| Patrick | | | | | |
| Ravi | | | | | |
| Peter | | | | | |

Challenges

- Constantly aware of software performance and processing benchmarks
- Has no time to learn new technologies that are critical to competitive development requirements

User Stories

- I want answers to specific software questions for the device I am programming
- I have to have quick access to software libraries, drivers, and firmware for my device
- I need to find the specific device I am programming and see all the support and documentation available

Job Goals

- Wants to design using familiar tools
- Cares about the availability of software drivers
- Expects a good set of debugging tools
- Seeks to influence embedded ecosystem selection process

Narrative

- Experience with embedded software development environment
- Limited or no direct experience with FPGAs
- Degree in CS or CE
- Software team influences vendor selection and selection of FPGAs verses other options

Trust Relationships

- Works closely with system architect and hardware designer
- Active in forums and LinkedIn developer groups
- Works with hardware designers to test software

David Chen



User Role: Architect
Group: Technology Group

Job Title: Architect
Reports to: Engineering Manager

Roles in Product Development Process

| | | | | | |
|--------------|--------------|--------------|----------------|--------------|---------|
| Tim | | | | | |
| Maddie | | | | | |
| David | | | | | |
| Patrick | | | | | |
| Ravi | | | | | |
| Peter | | | | | |
| | Requirements | Architecture | Implementation | Verification | Release |

Challenges

- Turn requirements into a workable architecture design
- Identifying technical risk areas and mitigating risk through modeling, analysis, simulations, and prototyping

User Stories

- I want to find and review reference designs for the devices I'm evaluating
- I want an advanced search function that can find alternate ways to implement my designs
- I need quick lookups for bandwidths, processing speeds, and IP blocks

Job Goals

- Establish the basic structure of the system, define the essential core design features and elements that provide a development framework
- Design models in a high-level language
- Influence the tools and IP libraries
- Manage costs and budget

Narrative

- Experience with both ASIC and FPGA designs
- Has a BSEE or MSEE degree
- 25 years + experience
- Proficiency in HDL programming, FPGA-based logic design, and timing analysis

Trust Relationships

- Works with software, design, implementation engineers, and RTL designers
- Attends technical conferences, such as Design West (ESC)

Patrick Smith



User Role: Engineer
Group: Technology Group

Job Title: Implementation Engineer
Reports to: Engineering Manager

Roles in Product Development Process

| | Requirements | Architecture | Implementation | Verification | Release |
|----------------|--------------|--------------|----------------|--------------|---------|
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| David | | | | | |
| Patrick | | | | | |
| Ravi | | | | | |
| Peter | | | | | |

Challenges

- Closure on all timing specifications
- Logic verification
- Design re-use
- May be asked to manage legacy code; and doesn't want to learn new tools

User Stories

- I need to find solutions to implementation problems, specifically for tool problems
- I need to find the correct IP with documentation and references
- I have to know the correct compilation times for the entire device
- I want easy access to all known issues, bugs, and errata

Job Goals

- Integrate the whole design, achieving timing closure and delivering the final FPGA design
- Become involved in the system design of the architecture from an FPGA/ASIC perspective
- Provide code documentation
- Want to influence FPGA/ASIC selection process

Narrative

- Experienced with HDL languages, Synthesis, Place and Route, and simulation tools
- Familiar with ASIC/FPGA architectures
- Understands timing closure issues and timing analysis
- BS or MS in EE or CE
- Background in ASIC or FPGA design
- May be more junior and without RTL expertise

Trust Relationships

- Meets with FPGA/ASICS vendors throughout design cycles
- Interacts with systems architect, design manager, integrator engineer, verification engineer

Ravi Shukla



Job Title: Verification Engineer
 Reports to: Engineering Manager

Roles in Product Development Process

| | | | | | |
|-------------|--------------|--------------|----------------|--------------|---------|
| Tim | | | | | |
| Maddie | | | | | |
| David | | | | | |
| Patrick | | | | | |
| Ravi | | | | | |
| Peter | | | | | |
| | Requirements | Architecture | Implementation | Verification | Release |

User Role: Engineer
 Group: Technology Group

Challenges

- Verification processes and techniques
- Communication with systems architect
- Accurate runtime and test coverages

User Stories

- I need to find development kits and reference designs that match the devices we are verifying
- I need information and documentation to validate designs
- I need easy, quick access to known issues, bugs, and errata
- I want to know all characterization and packaging information

Job Goals

- Responsible for meeting end-system requirements and reliability
- Maintain an architect regression test infrastructure
- Influence the verification tool selection process
- Progress to simulation and on-chip debugging

Narrative

- Experienced with 3rd party EDA verification tools
- Experienced with FPGA tools
- Knowledge of HDL
- BS or MS in Engineering
- Background in system development

Trust Relationships

- Works with software and hardware developers
- Attends verification engineering conferences and seminars

Peter Branson



User Role: Designer
Group: Technology Group

Job Title: Board Designer
Reports to: Engineering Manager

Roles in Product Development Process

| | Requirements | Architecture | Implementation | Verification | Release |
|--------------|--------------|--------------|----------------|--------------|---------|
| Tim | | | | | |
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| David | | | | | |
| Patrick | | | | | |
| Ravi | | | | | |
| Peter | | | | | |

Challenges

- Update on device pin-outs and I/O standards, interfaces, voltage rails, and configuration schemes
- Design tools and specifications
- No formal education process for device knowledge and specifications
- Maintain signal Integrity
- Integration with PCB tools

User Stories

- I need to look up pin-out information, schematics and rules, SPICE models, and board design
- I need to gain experience with Quartus II and FPGA design standards
- I want to find board debug tools, data sheets, and pin connection guidelines

Job Goals

- Specialize in PCB schematic and layout, pin planning, system power and thermal design, and board bring-up and debug procedures
- Create PCB board schematic and perform PCB layout
- Responsible for board bring-up and debug
- Verification of board design

Narrative

- Experienced with 3rd party tools
- Experienced with FPGA tools
- BS or MS in Engineering
- May have experience with third-party EDA signal integrity tools
- Limited or no experience with Quartus II or FPGA design software and tools
- Familiar with test equipment (oscilloscopes, logic analyzers, network analyzers)

Trust Relationships

- Works with hardware system architect and developers
- Meets with device vendors, including FPGA vendors to ask questions
- Spends lots of time with Application Engineers working on customer solutions